SATISH NARAYANASAMY, Ph.D.

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Expertise: Computer architecture, Multicore Processors, Parallel Systems and Programming, Compilers and program analysis, Accelerators, Hardware enabled Security and Privacy, Parallel systems for genome sequencing, Memory and Network-on-Chip

EXECUTIVE PROFILE

Professor of Computer Science and Engineering with over 20 years of experience specializing in computer architecture, parallel systems and programming, accelerators, trustworthy computing, hardware security, and systems for genomics. Proven track record of translating complex architectural concepts into commercial reality, actively collaborating with leading technology firms including Google, NVIDIA, AMD, Microsoft, and Intel. Currently directs the KernelBridge project, that generates expert-level GPU parallel code from higher-level AI domain-specific languages. Foundational research in parallel computing, deterministic replay, and thread scheduling directly shaped industry-standard development and simulation tools (e.g., Intel PinPlay, Microsoft WinDbg iDNA). Hold Hall of Fame status across several flagship conferences: ISCA, ASPLOS, and PLDI.

LITIGATION SUPPORT & TECHNICAL CONSULTING

Technical Expert Witness | Hirambo Inc. v. Logic Solutions Inc. (Case 14-14236) | 2015

- Retained by Edward Allen Law on behalf of Hirambo, Inc. for a mobile software development dispute in the U.S. District Court for the Eastern District of Michigan.
- Conducted technical analysis, source-code review, and prepared expert reports.
- Evaluated source-code quality and assessments on industry-standard practices for software project management, software development, code writing, code reuse, and bug tracking.

Industry Collaborator & Consultant | Google, NVIDIA, AMD, Microsoft, Intel | 2003–Present

- Advise and collaborate with top-tier semiconductor and cloud computing corporations on cutting-edge multicore processors, systems reliability, parallel programming tools and analysis, and hardware-rooted security.
- Facilitate the transition of academic hardware/software theory into actionable corporate applications, influencing diagnostic and simulation tools (Intel PinPlay, Microsoft iDNA).

ACADEMIC & PROFESSIONAL EMPLOYMENT

University of Michigan, Ann Arbor

- Professor, Electrical Engineering and Computer Science (2020–Present)
- Associate Professor (2014–2020)
- Morris Wellman Assistant Professor (2008–2014)

Sequal Inc.

- CEO & Co-founder (2017–2020) — Directed a precision health startup focused on hardware-accelerated systems and sequencing.

Industry Research Appointments

- Microsoft Research, Bangalore: Consultant (2015)
- Microsoft Research, Redmond: Visiting Researcher (2007, 2013)
- Microsoft, Redmond: Intern, Center for Software Excellence (2006)
- Intel, Santa Clara: Intern, Microprocessor Research Lab (2003–2004)

HONORS & AWARDS

- ISCA Hall of Fame
- ASPLOS Hall of Fame
- PLDI Hall of Fame
- CACM Research Highlight: Awarded for 'GenDP' (2025)
- CoE Trudy Huebner Service Excellence Award (2024)
- ISCA 25-Year Retrospective: Selected for enduring impact for 'BugNet' (2023)
- IEEE Micro Top Picks Award (5x): Recognized for papers 'most relevant to industry' (2005, 2006, 2013, 2019, and Honorable Mention 2021)
- Best Paper Award, ISPASS (2019)
- Morris Wellman Faculty Development Professorship (2014)
- Google Research Faculty Award (2014)
- NSF CAREER Award (2012)
- Best Paper Award, ASPLOS (2011)
- Best Paper Nomination, DATE (2011)

PROFESSIONAL LEADERSHIP & INDUSTRY STANDING

- Vice Chair: ASPLOS (2027)
- Keynote Speaker: Recently delivered an invited keynote address at an ASPLOS Workshop
- Invited Delegate: 'Failure is not an option: Popular Parallel Programming', CRA-CCC Workshop (2010)
- Associate Editor: ACM Transactions on Computer Systems (2019–2022); IEEE Computer Architecture Letters (2017–2020)
- Program Co-Chair: WODA (2013)
- Program Committee Member (2008–Present): Routinely relied upon to peer-review cutting-edge research for leading international conferences, including ISCA, MICRO, ASPLOS, PLDI, HPCA, PPoPP, PACT, ISPASS
- Funding Panelist for 10+ panels: National Science Foundation
- University of Michigan Leadership: Faculty Search Committee Chair (Interviewed >150 candidates, hired >25 faculty)

EDUCATION

- Ph.D. in Computer Science, University of California, San Diego (2007)
  Dissertation: "Deterministic Replay Using Processor Support and Its Applications" (Advisor: Prof. Brad Calder)
- M.S. in Computer Science, University of California, San Diego (2005)
- B.E. in Computer Science and Engineering, Anna University, Chennai (2001)

TEACHING EXPERIENCE

University of Michigan, Ann Arbor

- **EECS 370: Introduction to Computer Organization**
  - Taught 14 sections (Most recent: Fall 2022)
- **EECS 570: Parallel Computer Architecture**
  - Most recent: Winter 2026
- **EECS 498/598: Hardware Accelerated Systems for AI and Health**
  - Fall 2019
- **EECS 497: Major Design Engineering**
  - Fall 2017
- **EECS 483: Compiler Construction**
  - Winter 2009, Winter 2010, Winter 2011, Winter 2013
- **EECS 598: Special Topics - Ubiquitous Parallelism**
  - Fall 2010, Winter 2012

PUBLICATIONS (Thematically Organized for Legal Relevance)

Google Scholar: ~6,000+ Citations | **h-index:** 35+

Security, Trustworthy Computing, Hardware-Rooted Security

- Jonah Rosenblum, Juechu (Joy) Dong, Peter M. Chen, Satish Narayanasamy. "Timelock Drive: Isolated Time-Based Defense for Storage Systems." *USENIX Symposium on Operating Systems Design and Implementation (OSDI)*, 2026.
- Jonah Rosenblum, Juechu (Joy) Dong, Satish Narayanasamy. "Confidential Computing for Population-Scale Genome-Wide Association Studies with SECRET-GWAS." *Nature Computational Science*, 2025.
- Kevin Loughlin, Ian Neal, Jiacheng Ma, Elisa Tsai, Ofir Weisse, Satish Narayanasamy, Baris Kasikci. "DOLMA: Securing Speculation with the Principle of Transient Non-Observability." *USENIX Security Symposium*, 2021.
- Shaizeen Aga, Satish Narayanasamy. "InvisiPage: Oblivious Demand Paging for Secure Enclaves." *International Symposium on Computer Architecture (ISCA)*, 2019.

- Subarno Banerjee, David Devecsery, Peter M. Chen, Satish Narayanasamy. "Iodine: Fast Dynamic Taint Tracking Using Rollback-free Optimistic Hybrid Analysis." *IEEE Symposium on Security and Privacy (S&P)*, 2019.
- Shaizeen Aga, Satish Narayanasamy. "InvisiMem: Smart Memory Defenses for Memory Bus Side Channel." *International Symposium on Computer Architecture (ISCA)*, 2017.
- Weihaw Chuang, Satish Narayanasamy, Brad Calder, Ranjit Jhala. "Bounds Checking with Taint-Based Analysis." *International Conference on High Performance Embedded Architectures and Compilers (HiPEAC)*, 2007.
- Weihaw Chuang, Satish Narayanasamy, Brad Calder. "Accelerating Meta Data Checks for Software Correctness and Security." *Journal of Instruction-Level Parallelism*, 2007.

Domain-Specific Accelerators for Genomics, Web, and Edge

- Reetuparna Das, Satish Narayanasamy. "Systems Challenges and Opportunities for Genomics." *Computer*, 2024.
- Gu et al. (including Satish Narayanasamy). "GenDP: A Framework of Dynamic Programming Acceleration for Genome Sequencing Analysis." *International Symposium on Computer Architecture (ISCA)*, 2023. (CACM Research Highlight 2025).
- Dunn, et al. (including Satish Narayanasamy). "SquiggleFilter: An Accelerator for Portable Virus Detection." *International Conference on Microarchitecture (MICRO)*, 2021.
- Zhehong Wang, et al. (including Satish Narayanasamy). "A 2.46M Reads/s Seed-Extension Accelerator for Next-Generation Sequencing Using a String-Independent PE Array." IEEE Journal of Solid-State Circuits, 2021.
- Arun Subramaniyan, et al. (including Satish Narayanasamy). "Accelerated Seeding for Genome Sequence Alignment with Enumerated Radix Trees." International Symposium on Computer Architecture (ISCA), 2021.
- Arun Subramaniyan, et al. (including Satish Narayanasamy). "GenomicsBench: A Benchmark Suite for Genomics." IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2021.
- Zhehong Wang, et al. (including Satish Narayanasamy). "A 2.46M reads/s Genome Sequencing Accelerator using a 625 Processing-Element Array." IEEE Custom Integrated Circuits Conference (CICC), 2020.

- Daichi Fujiki, et al. (including Satish Narayanasamy). "SeedEx: A Genome Sequencing Accelerator for Optimal Alignments in Subminimal Space." International Symposium on Microarchitecture (MICRO), 2020.
- Xiao Wu, et al. (including Satish Narayanasamy). "17.3 GCUPS Pruning-Based Pair-Hidden-Markov-Model Accelerator for Next-Generation DNA Sequencing." IEEE Symposium on VLSI Circuits, 2020.
- Hossein Golestani, Scott Mahlke, Satish Narayanasamy. "Characterization of Unnecessary Computations in Web Applications." *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, 2019.
- Daichi Fujiki, Arun Subramaniyan, Tianjun Zhang, Yu Zheng, Reetuparna Das, David Blaauw, Satish Narayanasamy. "GenAx: A Genome Sequencing Accelerator." *International Symposium on Computer Architecture (ISCA)*, 2018.
- Gaurav Chadha, Scott Mahlke, Satish Narayanasamy. "Accelerating Asynchronous Programs through Event Sneak Peek." *International Symposium on Computer Architecture (ISCA)*, 2015.
- Gaurav Chadha, Scott Mahlke, Satish Narayanasamy. "EFetch: Optimizing Instruction Fetch for Event-Driven Web Applications." *International Conference on Parallel Architectures and Compilation Techniques (PACT)*, 2014.

Memory Systems, Persistency, CXL, PIM, Microarchitecture

- Juechu Dong, Jonah Rosenblum, Satish Narayanasamy. "Toleo: Scaling Freshness to Tera-scale Memory Using CXL and PIM." *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2024.
- Vaibhav Gogte, William Wang, Stephan Diestelhorst, Peter M. Chen, Satish Narayanasamy, Thomas F. Wenisch. "Relaxed Persist Ordering Using Strand Persistency." *International Symposium on Computer Architecture (ISCA)*, 2020.
- Aasheesh Kolli, Vaibhav Gogte, Ali Saidi, Stephan Diestelhorst, William Wang, Peter M. Chen, Satish Narayanasamy, Thomas F. Wenisch. "Language Support for Memory Persistency." *IEEE Micro Top Picks*, 2019.
- Vaibhav Gogte, William Wang, Stephan Diestelhorst, Aasheesh Kolli, Peter M. Chen, Satish Narayanasamy, Thomas F. Wenisch. "Software Wear Management for Persistent Memories." *USENIX Conference on File and Storage Technologies (FAST)*, 2019.
- Aditya Narayan, Tiansheng Zhang, Shaizeen Aga, Satish Narayanasamy, Ayse Kivilcim Coskun. "MOCA: Memory Object Classification and Allocation in Heterogeneous Memory Systems." *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, 2018.

- Vaibhav Gogte, Stephan Diestelhorst, William Wang, Satish Narayanasamy, Peter M. Chen, Thomas F. Wenisch. "Persistency for Synchronization-Free Regions." *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, 2018.
- Aasheesh Kolli, Vaibhav Gogte, Ali Saidi, Stephan Diestelhorst, Peter M. Chen, Satish Narayanasamy, Thomas F. Wenisch. "Language-Level Persistency." *International Symposium on Computer Architecture (ISCA)*, 2017.
- Shaizeen Aga, Supreet Jeloka, Arun Subramaniyan, Satish Narayanasamy, David Blaauw, Reetuparna Das. "Compute Caches." *IEEE Symposium on High Performance Computer Architecture (HPCA)*, 2017.
- Reetuparna Das, Satish Narayanasamy, Sudhir Satapathy, Ron Dreslinski. "Catnap: Energy Proportional Multiple Network-on-Chip." *International Symposium on Computer Architecture (ISCA)*, 2013.
- Sujay Phadke, Satish Narayanasamy. "MLP-aware Heterogeneous Memory System." *Design, Automation & Test in Europe (DATE)*, 2011.
- Satish Narayanasamy, Hong Wang, Perry Wang, John Shen, Brad Calder. "A Dependency Chain Clustered Microarchitecture." *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, 2005.

Parallel Programming Model – Memory Consistency

- Daniel Marino, Abhayendra Singh, Todd D. Millstein, Madanlal Musuvathi, Satish Narayanasamy. "DRFx: An Understandable, High Performance, and Flexible Memory Model for Concurrent Languages." ACM Transactions on Programming Languages and Systems (TOPLAS), 2016.
- Abhayendra Singh, Shaizeen Aga, Satish Narayanasamy. "Efficiently enforcing strong memory ordering in GPUs." *International Conference on Microarchitecture (MICRO)*, 2015.
- Shaizeen Aga, Abhayendra Singh, Satish Narayanasamy. "zFence: Data-less Coherence for Efficient Fences." *International Conference on Supercomputing (ICS)*, 2015.
- Dan Marino, Todd Millstein, Madan Musuvathi, Satish Narayanasamy, Abhayendra Singh. "The Silently Shifting Semicolon." *Inaugural Summit on Advances in Programming Languages (SNAPL)*, 2015.
- Abhayendra Singh, Satish Narayanasamy, Dan Marino, Todd Millstein, Madan Musuvathi. "A Safety-First Approach to Memory Models." *IEEE Micro Top Picks*, 2013.

- Jessica Ouyang, Peter M. Chen, Jason Flinn, Satish Narayanasamy. "...and region serializability for all." *USENIX Workshop on Hot Topics in Parallelism (HotPar)*, 2013.
- Abhayendra Singh, Satish Narayanasamy, Dan Marino, Todd Millstein, Madan Musuvathi. "End-to-end Sequential Consistency." *International Symposium on Computer Architecture (ISCA)*, 2012.
- Abhayendra Singh, Dan Marino, Satish Narayanasamy, Todd Millstein, Madan Musuvathi. “Efficient processor support for DRFx, a memory model with exceptions." *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2011.
- Dan Marino, Abhayendra Singh, Todd Millstein, Madan Musuvathi, Satish Narayanasamy. "A Case for SC-preserving Compiler." *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, 2011.
- Dan Marino, Abhayendra Singh, Todd Millstein, Madan Musuvathi, Satish Narayanasamy. "DRFx: A Simple andcac Efficient Memory Model for Concurrent Programming Languages." *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, 2010.

Concurrency, Program Analysis & System Software

- David Devecsery, et al. "Optimistic Hybrid Analysis: Accelerating Dynamic Analysis through Predicated Static Analysis." *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2018.
- Chun-Hung Hsiao, Satish Narayanasamy, Essam Khan, Cristiano Pereira, Gilles Pokam. "AsyncClock: Scalable Inference of Asynchronous Event Causality." *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2017.
- Shaizeen Aga, Sriram Krishnamoorthy, Satish Narayanasamy. "CilkSpec: optimistic concurrency for Cilk." *International Conference for High Performance Computing, Networking, Storage and Analysis (SC)*, 2015.
- Chun-Hung Hsiao, Jie Yu, Satish Narayanasamy, Ziyun Kong, Cristiano L. Pereira, Gilles A. Pokam, Peter M. Chen, Jason Flinn. "Race Detection for Event-Driven Mobile Applications." *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, 2014.
- Chun-Hung Hsiao, Michael Cafarella, Satish Narayanasamy. "Reducing MapReduce Abstraction Costs for Text-Centric Applications." *International Conference on Parallel Processing (ICPP)*, 2014.

- Benjamin Wester, David Devecsery, Peter M. Chen, Jason Flinn, Satish Narayanasamy. "Parallelizing Data Race Detection." *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2013.
- Jie Yu, Satish Narayanasamy, Cristiano Pereira, Gilles Pokam. "Maple: A coverage-driven testing tool for multithreaded programs." *Conference on Object-Oriented Programming Systems, Languages, and Applications (OOPSLA)*, 2012.
- Gaurav Chadha, Scott Mahlke, Satish Narayanasamy. "When less is more (LIMO): Controlled parallelism for improved efficiency." *ACM International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, 2012.
- Kaushik Veeraraghavan, Peter M. Chen, Jason Flinn, Satish Narayanasamy. "Detecting and surviving data races using complementary schedules." *ACM Symposium on Operating Systems Principles (SOSP)*, 2011.
- Jie Yu, Satish Narayanasamy. "Tolerating Concurrency Bugs Using Transactions as Lifeguards." *International Symposium on Microarchitecture (MICRO)*, 2010.
- Daniel Marino, Madan Musuvathi, Satish Narayanasamy. "LiteRace: Effective Sampling for Lightweight Data-Race Detection." *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, 2009.
  Jie Yu, Satish Narayanasamy. "A Case for an Interleaving Constrained Shared-Memory Multi-Processor." *International Symposium on Computer Architecture (ISCA)*, 2009.
- Weihaw Chuang, Satish Narayanasamy, Ganesh Venkatesh, Jack Sampson, Michael Van Biesbrouck, Gilles Pokam, Osvaldo Colavin, Brad Calder. "Unbounded Page-Based Transactional Memory." *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2006.

Reliability, Forensics, Replay, Profiling

- Dongyoon Lee, Peter M. Chen, Jason Flinn, Satish Narayanasamy. "Chimera: Hybrid Program Analysis for Determinism." *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, 2012.
- Kaushik Veeraraghavan, Dongyoon Lee, Benjamin Wester, Jessica Ouyang, Peter M. Chen, Jason Flinn, Satish Narayanasamy. "DoublePlay: Parallelizing Sequential Logging and Replay." *ACM Transactions on Computer Systems (TOCS) / ASPLOS*, 2011.
- Dongyoon Lee, Mahmoud Said, Satish Narayanasamy, Zijiang Yang. "Offline symbolic analysis to infer Total Store Order." *IEEE International Symposium on High Performance Computer Architecture (HPCA)*, 2011.

- Dongyoon Lee, Benjamin Wester, Kaushik Veeraraghavan, Satish Narayanasamy, Peter M. Chen, Jason Flinn. "Respec: Efficient Online Multiprocessor Replay via Speculation and External Determinism." *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2010.
- Jessica Ouyang, Kaushik Veeraraghavan, Dongyoon Lee, Peter M. Chen, Jason Flinn, Satish Narayanasamy. "Epoch parallelism: One execution is not enough." *USENIX Workshop on Hot Topics in Parallelism (HotPar)*, 2010.
- Dongyoon Lee, Mahmoud Said, Satish Narayanasamy, Zijiang Yang, Cristiano Pereira. "Offline Symbolic Analysis for Multi-Processor Replay." *International Symposium on Microarchitecture (MICRO)*, 2009.
- Satish Narayanasamy, Ayse Coskun, Brad Calder. "Transient fault prediction based on anomalies in processor events." *Design, Automation, and Test in Europe (DATE)*, 2007.
- Satish Narayanasamy, Zhenghao Wang, Jordan Tigani, Andrew Edwards, Brad Calder. "Automatically Classifying Benign and Harmful Data Races Using Replay Analysis." *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, 2007.
- Satish Narayanasamy, Cristiano Pereira, Brad Calder. "Recording Shared Memory Dependencies Using Strata." *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2006.
- Smruthi Sarangi, Satish Narayanasamy, Bruce Carneal, Abhishek Tiwari, Brad Calder, Josep Torrellas. "Patching Processor Design Errors Using Programmable Hardware." *IEEE Micro Top Picks 2007 (originally appeared in ICCD 2006).*
- Satish Narayanasamy, Cristiano Pereira, Brad Calder. "Software Profiling for Deterministic Replay Debugging of User Code." *International Conference on Software Methodologies, Tools and Techniques (SOMET)*, 2006.
- Satish Narayanasamy, Cristiano Pereira, Harish Patil, Robert Cohn, Brad Calder. "Automatic Logging of Operating System Effects to Guide Application-Level Architecture Simulation." *Joint International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS)*, 2006.
- Satish Narayanasamy, Gilles Pokam, Brad Calder. "BugNet: Continuously Recording Program Execution for Deterministic Replay Debugging." *International Symposium on Computer Architecture (ISCA)*, 2005.
- Satish Narayanasamy, Yuanfang Hu, Suleyman Sair, Brad Calder. "Creating Converged Trace Schedules Using String Matching." *International Symposium on High Performance Computer Architecture (HPCA)*, 2004.

- Satish Narayanasamy, Timothy Sherwood, Suleyman Sair, Brad Calder, George Varghese. "Catching Accurate Profiles in Hardware." *International Symposium on High Performance Computer Architecture (HPCA)*, 2003.

Genomics Software Systems

- Juechu Dong, Xueshen Liu, Harisankar Sadasivan, S Sitaraman, Satish Narayanasamy. "mm2-gb: GPU Accelerated Minimap2 for Long Read DNA Mapping." *ACM Conference on Bioinformatics, Computational Biology, and Health Informatics (ACM BCB)*, 2024.
- Harisankar Sadasivan, et al. (including Satish Narayanasamy). "The Genomic Computing Revolution: Defining the Next Decades of Accelerating Genomics." IEEE High Performance Extreme Computing Conference (HPEC), 2024.
- Tim Dunn, et al. (including Satish Narayanasamy). "Jointly benchmarking small and structural variant calls with vefdist." *Genome Biology*, 2024.
- Vishwaratn Asthana, et al. (including Satish Narayanasamy). " Development of a Rapid, Culture-Free, Universal Microbial Identification System Using Internal Transcribed Spacer Targeting Primers." *Journal of Infectious Diseases*, 2025.
- Tim Dunn, Satish Narayanasamy. "vefdist: Accurately benchmarking phased small variant calls in human genomes." *Nature Communications*, 2023.
- Tim Dunn, David T. Blaauw, Reetuparna Das, Satish Narayanasamy. "nPoRe: n-Polymer Realigner for improved pileup-based variant calling." *BMC Bioinformatics*, 2023.
- Harisankar Sadasivan, Milos Maric, Eric Dawson, Vishanth Iyer, Johnny Israeli, Satish Narayanasamy. "Accelerating Minimap2 for accurate long read alignment on GPUs." *Journal of Biotechnology and Biomedicine*, 2023.

Machine Learning and AI Systems

- Matthew Tomei, et al. (including Satish Narayanasamy). "Sensor Training Data Reduction for Autonomous Vehicles." HotEdgeVideo Workshop at *ACM Annual International Conference on Mobile Computing and Networking (MobiCom)*, 2019.
- Chun-Hung Hsiao, Michael Cafarella, Satish Narayanasamy. "Using Web Corpus Statistics for Program Analysis." *ACM SIGPLAN Conference on Object-Oriented Programming, Systems, Languages and Applications (OOPSLA)*, 2014.

PATENTS

- **Granted Patents**
  - **Trusted Computing System with Enhanced Memory** *US Patent 10,496,552* (Granted: Dec 2019)
  - **Ordering Constraint Management within Coherent Memory Systems** *US Patent 9,367,461* (Granted: Jun 2016)
  - **Sampling Techniques for Dynamic Data-Race Detection** *US Patent 8,418,146* (Granted: Apr 2013)
  - **Machine Instruction Level Race Condition Detection** *US Patent 7,861,118* (Granted: Dec 2010)
  - **System, Method and Apparatus for Dependency Chain Processing** *US Patent 7,603,546* (Granted: Oct 2009)

- **Published Patent Applications**
  - **Instruction Ordering** *WO Patent App. 2020/183119* (Published: Sep 2020)
  - **Efficient Seeding for Read Alignment** *US Patent App. 2020/0265923* (Published: Aug 2020)
  - **Evaluating Optimality of a Trace Generated During Sequence Alignment** *US Patent App. 2020/0234796* (Published: Jul 2020)
  - **Pruning Pair-HMM Algorithm and Hardware Architecture** *US Patent App. 2020/0234795* (Published: Jul 2020)

SOFTWARE ARTIFACTS

Concurrency Bug Detection & Testing

- **Maple:** A coverage-driven testing tool designed to systematically explore thread interleavings and expose hidden concurrency bugs.

Parallel Programming Memory Models & Compiler Infrastructure

- **SC-Preserving Compiler:** A compiler infrastructure designed to enforce Sequential Consistency (SC) end-to-end, preventing standard compiler optimizations from introducing memory model violations in concurrent code.

Parallel Record & Replay / Deterministic Execution

- **Intel PinPlay:** A widely adopted framework for the deterministic record and replay of multithreaded programs, utilized heavily for architectural simulation and software debugging.

- **iDNA (Microsoft WinDbg Integration):** Used load-value logging solution from BugNet. Record-and-replay research enabled classifying benign and harmful data-races.

Bioinformatics, Genomics & Hardware Accelerators

- **VCFdist (2023):** A tool for accurately benchmarking and evaluating phased small variant callers in human genomes.
- **nPore (2023):** An *n*-Polymer Realigner for improved pileup-based long-read variant calling.

- **BWA-MEM2 ERT (2021):** An optimized system for short-read whole genome sequencing (WGS).
- **SquiggleFilter (2021):** A hardware accelerator designed for portable, real-time virus detection.
- **GenomicsBench (2021):** A comprehensive benchmark suite for evaluating the performance of genomics systems and accelerators.

Research Funding & Industry Grants

- **Federal & Agency Grants**
  - **National Science Foundation (NSF) SHF Medium:** "Custom Computing for Genome Sequencing" (2024–2028) | *Principal Investigator* ($900,000)
  - **National Science Foundation (NSF) SHF Medium:** "Optimistic Static Analysis" | *Principal Investigator* ($1,079,989)
  - **National Science Foundation (NSF) CAREER Award:** "Holistic System Solutions for Empowering Parallel Programmers" | *Principal Investigator* ($538,671)
  - **National Science Foundation (NSF) SHF Small:** "Accelerating Asynchronous Programs through Synergistic Hardware/Software Customization" | *Principal Investigator* ($450,000)
  - **National Science Foundation (NSF) CSR Medium:** "Improving Software Reliability and Security through Multicore Technology" | *Co-Principal Investigator* ($1,200,000)
  - **National Science Foundation (NSF) SHF Small:** "Interleaving Constrained Parallel Runtime System for Tolerating Concurrency Bugs" | *Principal Investigator* ($499,946)
  - **DARPA / MARCO:** Center for Future Architecture Research | *Principal Investigator* ($300,000)

- **Industry Awards & Strategic Collaborations**
  - **Google:** Parallel programming for TPUs ($50,000)
  - **AMD:** Long Read Alignment ($30,000).
  - **Google:** Google Research Faculty Award ($75,000).
  - **Intel Corporation:** Over $275,000 in funded research and equipment grants focusing on parallel programs, event-driven systems ("Taming Concurrency in Event-Driven Systems"), and medical imaging applications.
  - **Microsoft:** Multiple research gifts and consulting engagements supporting academic research in parallel execution and hardware capabilities.